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AD A111986

VLSI ARRAY PROCESSOR

R&D STATUS REPORT

DARPA ORDER NO. 4001

CONTRACT NO. N00014-80-C-0693

CONTRACT DATE: August 1, 1980

PRINCIPAL INVESTIGATOR: Ed Greenwood

PHONE: (602)949-3349

JANUARY 11, 1982

REPORTING PERIOD - Thru December 31, 1981

APPROVED BY: Dale L. Fadley
Dale Fadley
Section Manager
Tactical Secure Systems

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MoTorola, Inc
Scottsdale, AZ

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Detail design of the Arithmetic Processor Unit (APU) chip has been completed. All cell types (100) have been run through the design rule check (DRC) programs, corrected and verified. DRC runs on the entire chip have been run and all corrections have been made. Fifteen out of eighteen of the chip DRC corrections have been verified. The metal, polysilicon and information data layers of the APU layout is shown in Figure 1. Figure 2 is a high level chip plan. The attached drawings, titled "VLSI Array Processor Arithmetic Processor Unit Chip Plan" is a detail drawing of the APU Chip Plan. Completion of design checks will be accomplished by January 15, 1982. Then the APU chip data base will be sent to MICARL for shrink to 3 micron rules (design was done in 4 micron rules) and compensation before initiating mask fabrication.

The functional level simulator of the APU has been built and verified using a set of APU diagnostic code. A gate level logic simulation of the APU has been built. The same set of APU Diagnostic Code is in integration and checkout of the APU logic simulator. This integration and test task is approximately 25% complete. This task will be completed before January 31, 1982.

The APU breadboard modules have been fabricated and check out has been initiated. The Array Processor Demonstration System (APDS) modules are in the wire-wrap process.

The APDS and APU microcode assembler have been built and checked out. The linker and loader for the APDS have also been built. The APDS simulator is approximately 75% built.

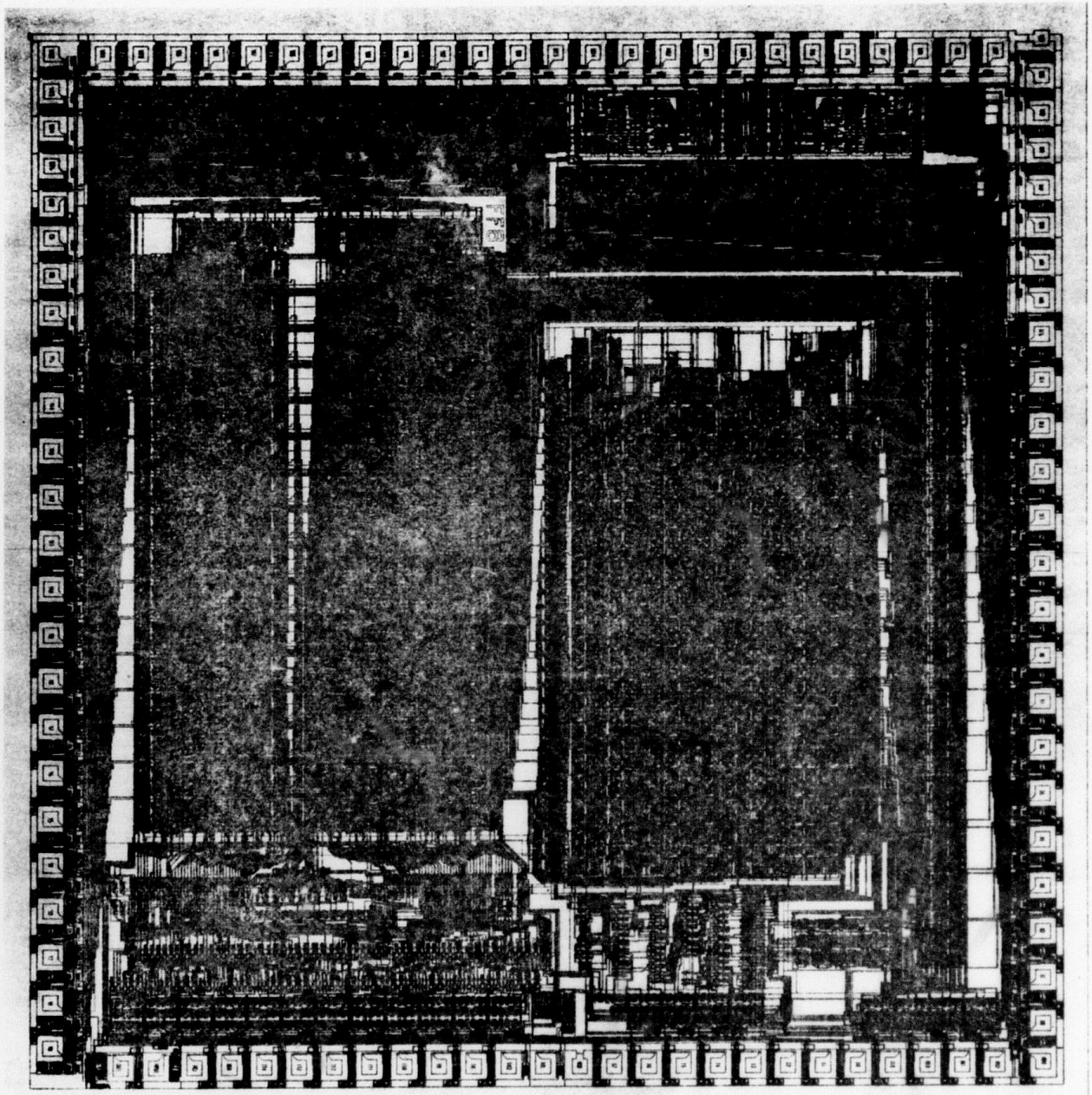

FIGURE 1
APU LAYOUT

Accession For
NTIS GRA&I
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By
Distribution/
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Dist | Avail and/or Special
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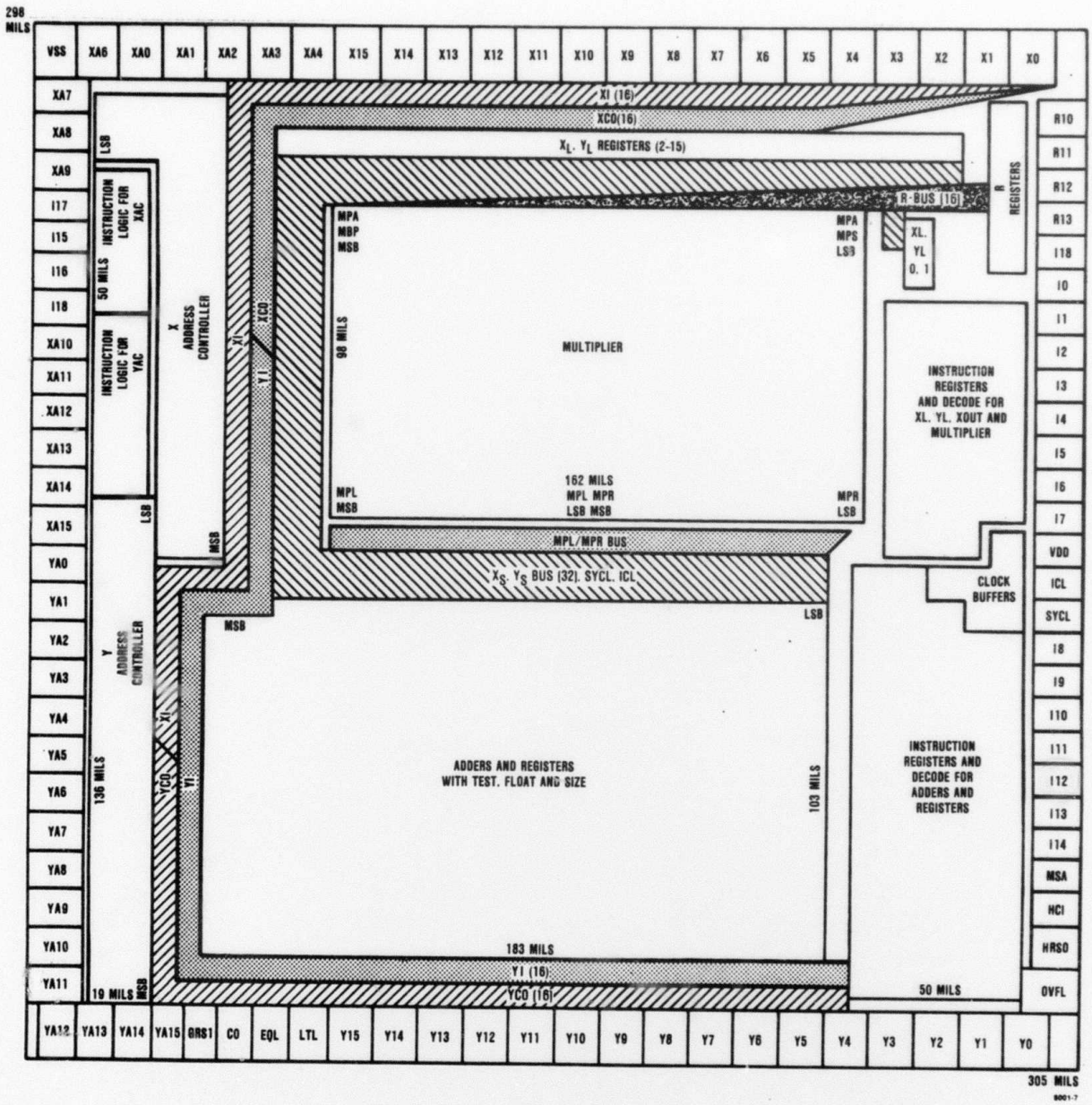


FIGURE 2

APU CHIP PLAN

The Architecture Report is being focused on and will be submitted to DARPA for review by January 31, 1982.

In the following quarter, the following activities are planned:

1) Complete VLSI APU design checks and deliver data base to MICARL
2) Fabricate APU mask set
3) Complete APDS simulator
4) Complete fabrication of APDS
5) Check out APU and APDS breadboards
6) Complete and deliver Interim Report (Architecture Report)

No technical problems are forseen at this time. A funds expenditure report is provided in Table I.

Date Prepared January 12, 1982
Contract No. N00014-80-C-0693
Contractor Motorola, Inc. GED

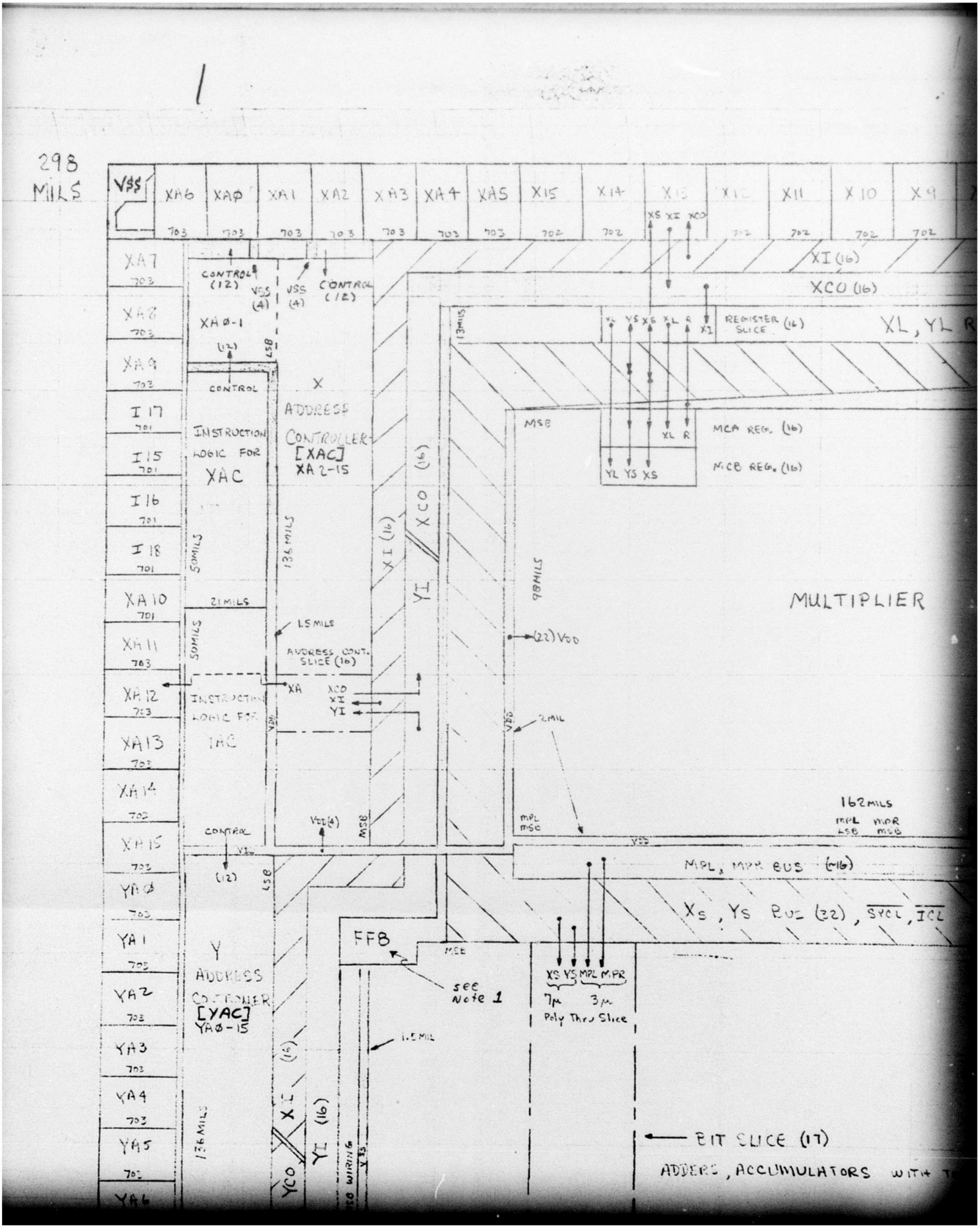
TABLE I

FUNDS EXPENDITURE REPORT

Summary Work Package Title Array Processor
Report Month December 1981

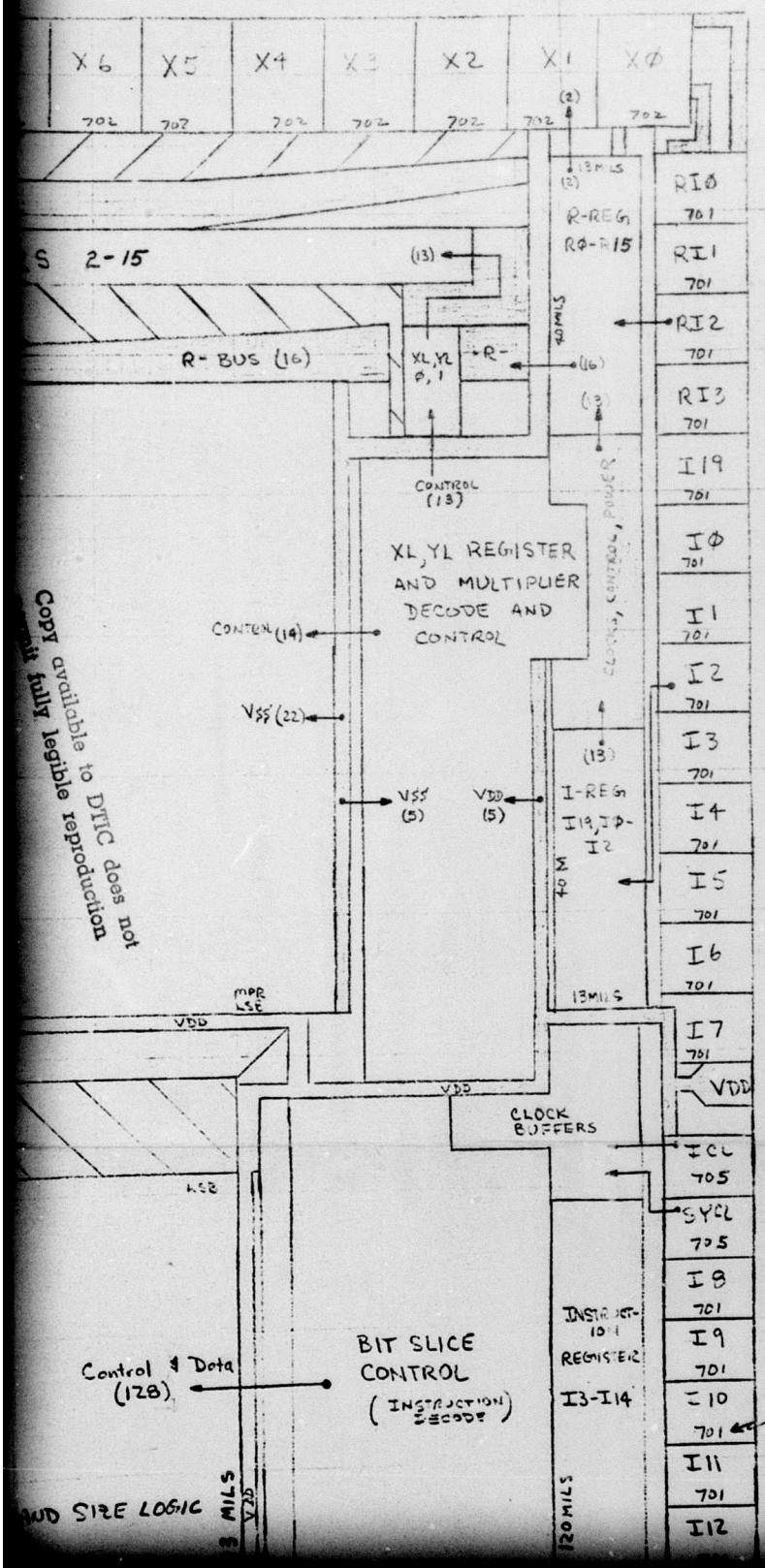
Column A ORIGINAL PROPOSAL	Column B Latest Accepted Revised Proposals (if any)	Column C Reporting Month Expenditures	Column D Cumulative Expenditures To Date			Column E Cost Complete estimate ••	Column F Latest Cost Estimate (D2 plus E) ••
			D1 Total Man Hours	D2 Dollar Value	D3* Percentage Dollar Value		
1. DIRECT LABOR							
Type No. of Hours@ Hourly Rate Dollar Total							
Total Direct Labor 161,363		9,777	11,903	175,551		80,457	256,008
Overhead 155,230		10,709		168,767		76,010	244,777
Total direct labor & O'Head 316,593		20,486		344,318		156,467	500,785
2. MATERIALS & PARTS 500,256		---		325,297		262,477	587,774
3. TRAVEL EXPENSE 20,120		667		9,581		13,026	22,607
4. COST OF MONEY 9,900		960		18,275		10,775	29,050
5. GEN & ADMN 156,938		8,497		129,194		77,804	206,998
6. OTHER COSTS 86,193		1,766		45,258		36,049	81,307
TOTAL COSTS 1,090,000		32,376		871,923	80.0	556,598	1,428,521
7. FIXED FEE (OR PROFIT) 99,000		2,941		79,193	80.0	19,807	99,000
TOTAL CONTRACT PRICE 1,189,000		35,317		951,116	80.0	576,405	1,527,521
***OUTSTANDING COMMITMENTS --		--		42,734	--	(42,734)	--
TOTAL COMMITMENTS AND EXPENDITURES 1,189,000		35,317		993,850		533,671	1,527,521

6


298 MILS
VSS
XA6
XAØ
XA1
XA2
XA3
XA4
XA5
X15
X14
X13
X12
X11
X10
X9
XS XI XCO
XA7
XA8
XA9
I17
I15
I16
I18
XA10
XA11
XA12
XA13
XA14
XA15
YAØ
YA1
YA2
YA3
YA4
YA5
YA6
CONTROL (12)
VSS (4)
XAØ-1
CONTROL
INSTRUCTION LOGIC FOR XAC
X ADDRESS CONTROLLER [XAC] XA2-15
50MILS
136MILS
21MILS
1.5MILS
ADDRESS CONT. SLICE (16)
XA
XCO
XI
YI
INSTRUCTION LOGIC FOR YAC
VDD
VDD(4)
MSB
CONTROL
(12)
LSB
Y ADDRESS CONTROLLER [YAC] YAØ-15
136MILS
YCO
XI (16)
YI (16)
XI (16)
XCO (16)
YI
13MILS
XCO (16)
XL YS XS XL R XI
REGISTER SLICE (16)
XL, YL R
MSB
XL R
MCA REG. (16)
YL YS XS
MCB REG. (16)
98MILS
(22) VDD
MULTIPLIER
2MIL
162MILS
MPL MSB
MPL MPR LSB MSB
VDD
MPL, MPR BUS (16)
XS, YS BUS (32), SYCL, ICL
FF8
see Note 1
XS YS MPL MPR
7μ 3μ
Poly Thru Slice
1.5MIL
LSB WIRING
VSS
BIT SLICE (17)
ADDERS, ACCUMULATORS WITH T

2

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	1	UPDATE LAYOUT	12/9/91	D.N.
	2	Documentation clean-up	12/9/91	E.G.



Notes:
1. FF8 is mask set identifier
2. 701 numbers refer to type of I/O cell
3. M is mils
4. (#) is the number (#) of lines
5. poly is run vertical thru cells; metal is run horizontal thru cells

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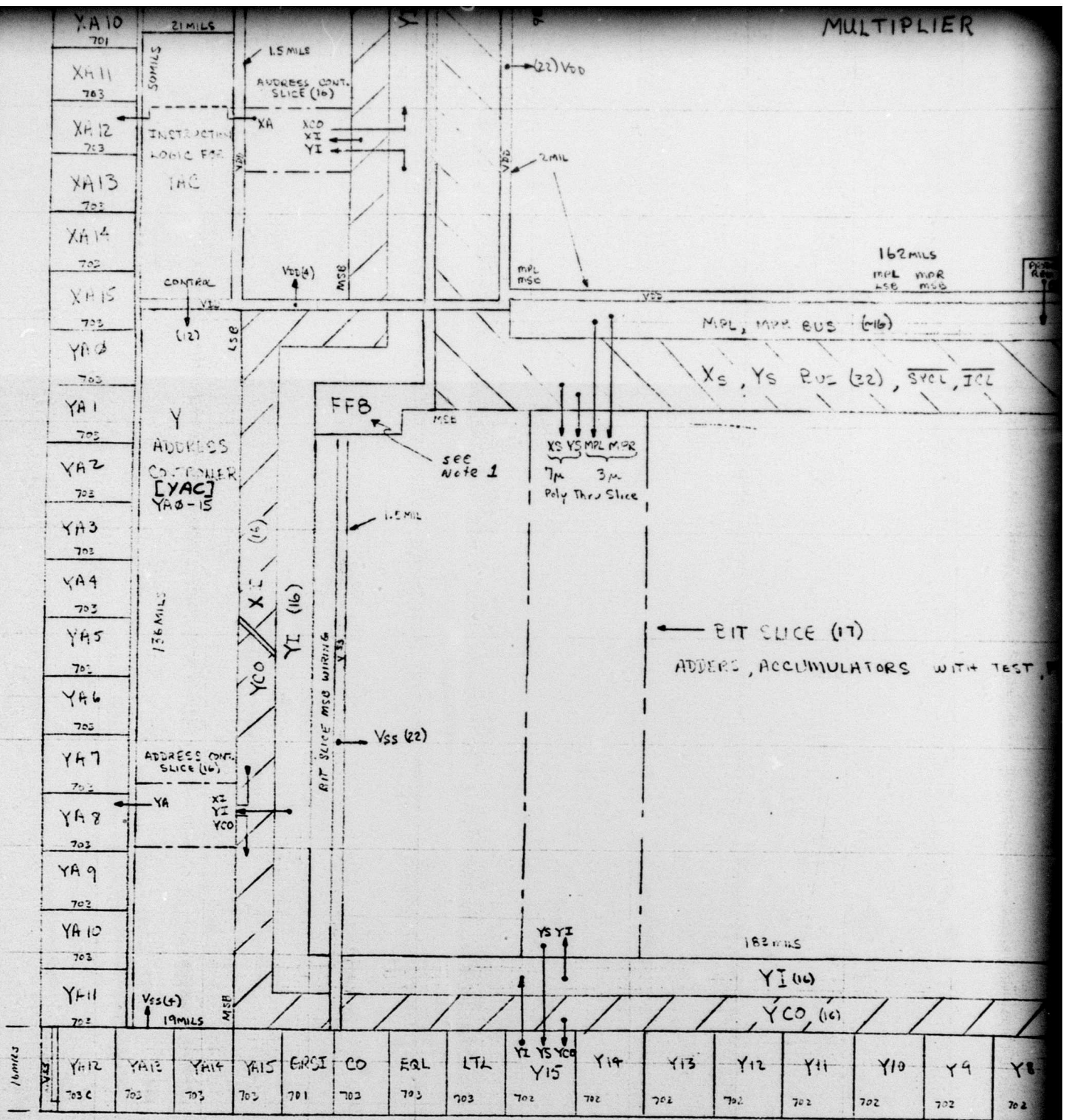
MULTIPLIER
XA10
701
21 MILS
XA11
703
XA12
703
XA13
703
XA14
703
XA15
703
YA0
703
YA1
703
YA2
703
YA3
703
YA4
703
YA5
703
YA6
703
YA7
703
YA8
703
YA9
703
YA10
703
YA11
703
50 MILS
1.5 MILS
ADDRESS CONT. SLICE (16)
XA
INSTRUCTION LOGIC FOR IMC
XCO
XI
YI
(22) VDD
2 MIL
162 MILS
MPL LSB
MPR MSB
MPL MSB
CONTROL
(12)
LSB
VDD(4)
MSB
VSS
MPL, MPR BUS (16)
XS, YS BUS (32), SYCL, ICL
Y ADDRESS CONTROLLER [YAC] YA0-15
FF8
MSB
see Note 1
XS YS MPL MPR
7μ 3μ
Poly Thru Slice
1.5 MIL
136 MILS
XI (16)
YI (16)
YCO
BIT SLICE MSB WIRING
BIT SLICE (17)
ADDERS, ACCUMULATORS WITH TEST,
VSS (22)
ADDRESS CONT. SLICE (16)
YA
XI
YI
YCO
YS YI
182 MILS
YI (16)
YCO (16)
VSS(4)
19MILS
MSB
16 MILS
YA12 703C
YA13 703
YA14 703
YA15 703
ERROR 701
CO 703
EQL 703
LTL 703
YI YS YCO Y15 702
Y14 702
Y13 702
Y12 702
Y11 702
Y10 702
Y9 702
Y8 702

3

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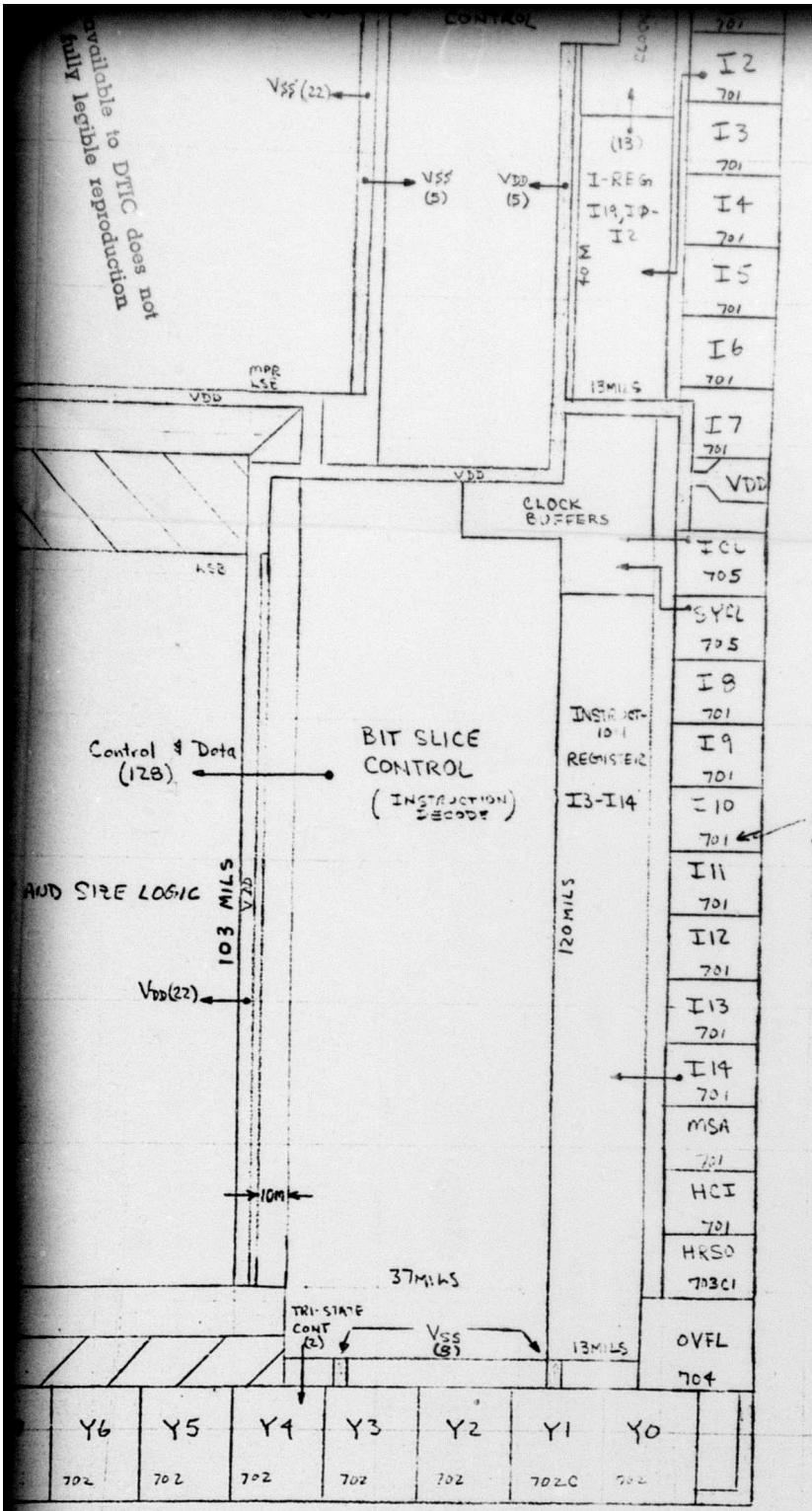

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DWN BY DAVE HARRISON	MOTOROLA Government Electronics Division 8201 E. McDOWELL ROAD, P.O. BOX 1417, SCOTTSDALE, ARIZONA 85252	
DOC CHK BY		
DSGN CHK BY		
MFG	VLSI ARRAY PROCESSOR	
PROJ NO. 3543-150	ARITHMATIC PROCESSOR UNIT	
CONTR NO	CHIP PLAN	
ISSUED 9-17-81	SIZE	FSCM NO. 94990
APVD	DWG NO.	
APVD	SCALE 50X	SHEET 1 of 1

305 MILS

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